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S-band Transmitter (STX) Interface Control Document

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Document Control

Rev.	Date	Section	Description of Change	Reason for Change
1.0	6 Dec 2013	All	First Release	
1.1	5 Feb 2014	All	Second Release	Update to connection diagram

Revision Control

Product	Part Number	Revisions Covered	Notes
STX	CPUT-STX-01	1.7	This documentation relates to the STX

Related Documents

No.	Document Name	Document Reference
CPUT-UM-STX-01	User Manual: S-band Transmitter (STX)	Revision 1.6

Contents

List of Figures

List of Tables

Nomenclature

Abbreviations

CSK	CubeSat Kit
FPGA	Field Programmable Gate Array
OBC	On-board computer
PA	Power Amplifier
STX	S-band Transmitter
TBC	To be confirmed
TR	Transmit ready

1 Introduction

2 Top Level Description

2.1 Overview

The STX is an integrated RF data transmitter module operating in the S-band and supporting data rates of up to 2 Mbps. This document describes the interfaces between the transmitter and an OBC via the PC/104 header stack connector. A general overview of the intended operation for the transmitter is provided. Operation is subject to change without notice.

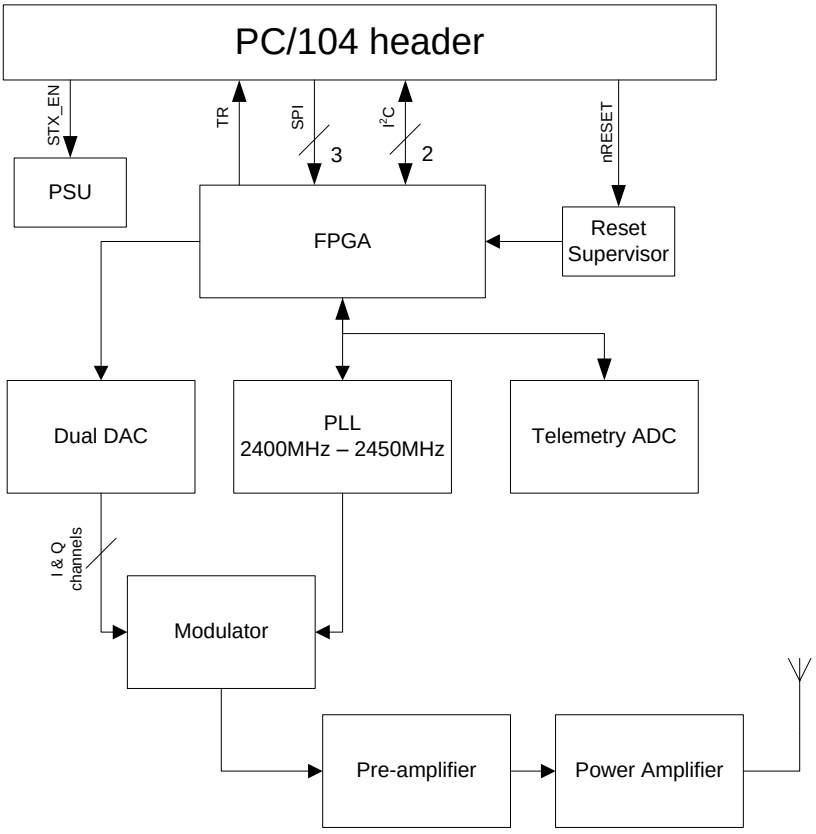

Figure 1: Block diagram of the STX with its CSK header connections

- Small form factor (CubeSat Kit PC/104 compatible)
- QPSK/OQPSK modulation schemes
- 2 Mbps data rate
- IntelSAT-308 based encoding
- Operation in Earth Exploration Satellite Services or amateur bands (built to order)

- Adjustable RF output power
- Adjustable data rate
- Simple digital interfaces
  - I^2C interface for Control/Telemetry
  - SPI interface for user data

2.2 Detailed Characteristics

2.2.1 Power

- Transmit RF output power maximum 30 dBm
- DC power consumption less than 6 W
- Compatible with Clyde Space EPS
  - Battery bus (6V – 12V)

2.2.2 RF

- Amateur band transmit frequency range 2400 MHz – 2450 MHz
- Carrier frequency adjustable in 500 kHz steps via I^2C telecommand
- Transmit RF output power adjustable to 21, 24, 27, 30 dBm

2.2.3 Encoding and modulation

- QPSK and OQPSK modulation schemes
- Open Network Encoding scheme based on IntelSAT IESS-308 specifications
- V.35 IntelSAT scrambler
- Differential encoding
- Half rate convolutional encoding (K=7)
- Pulse shaping filter (0.35 roll-off factor)
- 2 Mbps data rate with full, 1/2, 1/4, and 1/8 data rate modes

2.2.4 Physical

- Mass
  - < 95 g
- Form factor
  - 96×90.2×17 mm PC/104 CubeSat Kit compatible PCB
- Operating temperature range
  - $-25°C$ to $+61°C$

2.3 Detailed Description

2.3.1 FPGA

The STX utilises an Actel Igloo Nano FPGA for all data processing, encoding, and control. The FPGA's tolerance to single event upsets and radiation in low Earth orbit have made it a suitable candidate for this purpose. All the code modules were implemented in VHDL.

2.3.2 FPGA Support Circuitry

The FPGA is supported by a reset supervisor IC. The device monitors the supply voltage of the FPGA and will hold the FPGA in reset if there is an undervoltage condition. The reset supervisor will hold the FPGA in reset for 200 ms upon startup. An oscillator, to provide a clock signal to the FPGA is also included.

2.3.3 Sensors

The STX includes on-board temperature, current, and voltage sensors. All the sensor readings are provided as telemetry and are accessible via I^2C.

3 Mechanical interfaces

3.1 Specifications

Table 1: Mechanical specifications

	Value	**Units**
Dimensions	$96 \times 90.2 \times 17$	mm
Mass	< 95	g

3.2 Mechanical configuration

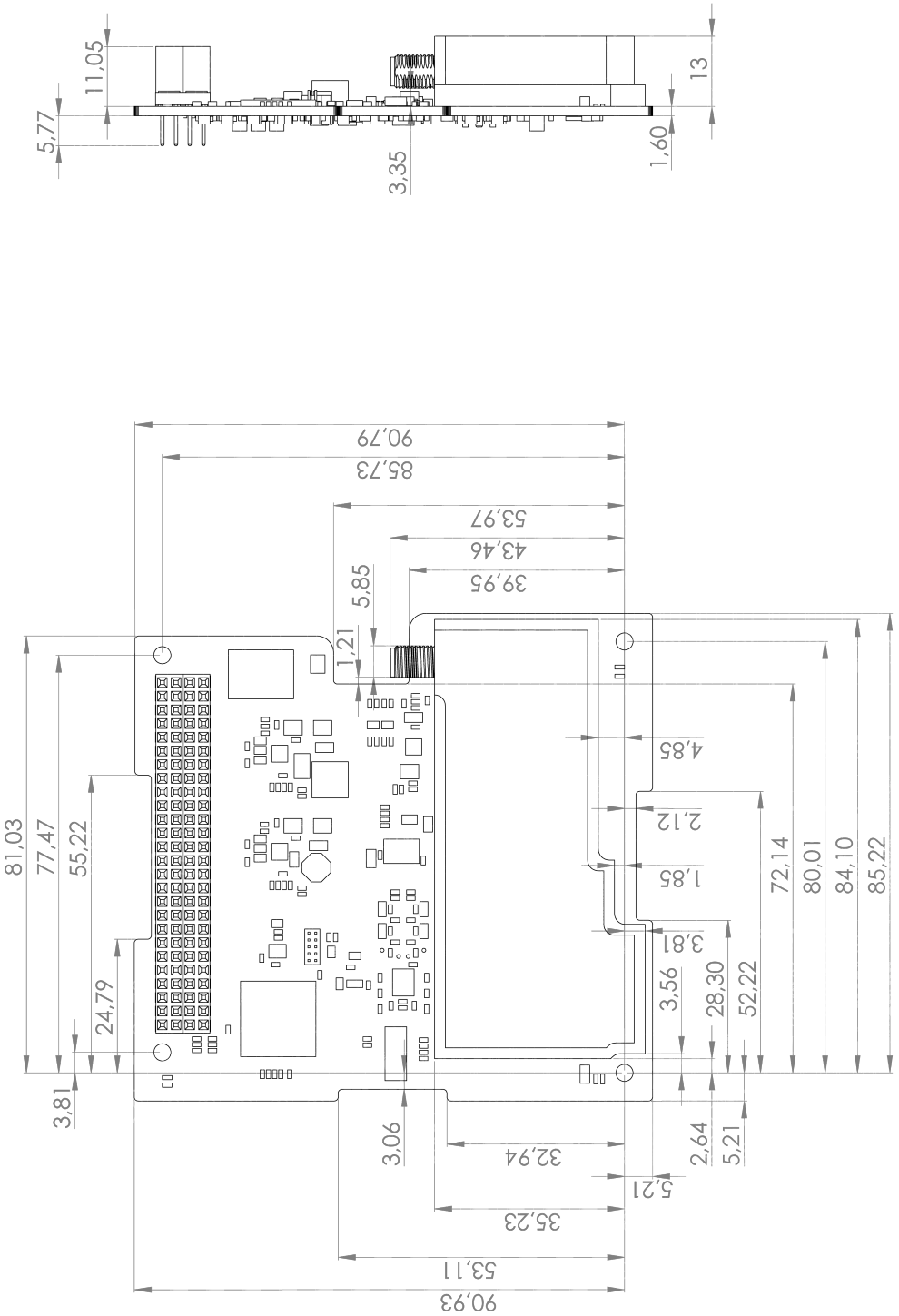

Figure 2: Mechanical diagram (shown in mm) [ESQ-126-13-G-D header shown]

3.3 Materials

Table 2: Materials list

Material	Manufacturer	%TML	%CVCM	%WVR	Application	Note
Scotch-Weld 2216 Epoxy B/A	3M	0.97	0.02	0.32	Adhesive Fixing	
					Conformal	
PCB Material	FR4	0.62	0	0.1	PCB Board	NASA Worst Case
Solder Resist	CARAPACE EMP110	0.95	0.02	0.31	Solder Mask	
Solder	Sn63					

3.4 Connectors

The STX utilises a 50 Ω SMA as the RF transmit connector. The STX header is a SAMTEC connector from the ESQ-1 range.

3.5 CSK header connections

Figure 3 illustrates the connections that are made available at the CSK header. Optional connections that are provided on the header include an FPGA reset, STX enable, SPI, transmitter buffer ready and alternative I^2C. The optional connections may be selected at the time of production and should be selected according to application and performance requirements. Either the primary I^2C or alternate I^2C must be chosen, not both. Should the optional functionality not be required it will not be made available at the header (there will be no physical connection). All signal voltage levels are 3.0 V LVCMOS, yet are 3.3 V compatible.

Pin #	Pin name	I/O type	Description	Optional
H1-41	SDA	Bidirectional	I^2C serial data	Yes*
H1-43	SCL	Input	I^2C serial clock	Yes*
H1-23	SDA_ALT	Bidirectional	Alternate I^2C data	Yes*
H1-21	SCL_ALT	Input	Alternate I^2C clock	Yes*
H1-13	TR	Output	Transmitter ready for data	Yes
H1-09	COMM_SCLK	Input	SPI clock	Yes
H1-11	COMM_MOSI	Input	SPI data	Yes
H1-12	COMM_CS	Input	SPI chip select	Yes
H1-15	nFPGA_RESET	Input	FPGA reset (active low)	Yes
H1-10	STX_EN	Input	Board power enable	Yes
H2-45	VBATT_BUS	Power	Battery bus supply	No
H2-46	VBATT_BUS	Power	Battery bus supply	No
H2-29	GND	Power	Power ground	No
H2-30	GND	Power	Power ground	No
H2-32	GND	Power	Power ground	No

Table 3: CSK connector pinouts

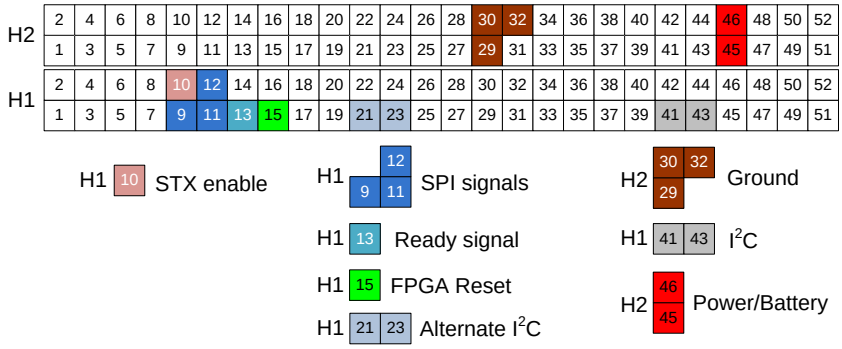

Figure 3: CSK header connections

4 Software interfaces

4.1 SPI

The high-speed SPI interface is utilised to transfer user data (payload data) to the STX. The serial data (MOSI) is sampled on the rising edge of the SPI clock (SCK).

- Mode 0
- CPOL = 0 (polarity)
- CPHA = 0 (phase)

4.2 I^2C operation

All telecommands and telemetry are communicated via I^2C. The default I^2C address is 0×26, but may be configured according to user specifications at time of production. Issuing a telecommand (writing data) has the following procedure. The first byte written to the I^2C points to the address of the register, and the following byte writes the value to the register. Reading telemetry follows a similar approach, firstly a byte is written to point to the correct register followed by a read transaction to return the value. Consecutive read transactions automatically increment the read pointer.

4.3 Operation

On power-up the STX is ready to transmit data. It will boot up with default settings for the data rate, RF power setting, etc.

Transmit

Data to be transmitted is sent via SPI. Each byte of data sent to the STX will be placed into the 4096 byte buffer. A transmit ready (TR) flag is provided to the PC/104 header as a hard signal (optional) as well as via an I^2C telemetry channel as a soft signal. The hard TR signal should provide a performance advantage as opposed to polling the I^2C telemetry channel since it can be used to interrupt an OBC. The TR flag will become active once the number of bytes in the buffer drops below a predefined threshold indicating more data can be added to the buffer. The threshold trigger for the TR flag has been configured to 513 bytes.

Sync bytes

The OBC may send a telecommand to put the STX into Synchronisation Mode. In this mode, when the PA is activated, synchronisation bytes will be sent from the transmitter (no real data is read from the SPI input data FIFO). This allows the ground station receiver to achieve lock (synchronisation) before actual payload data is transmitted over the link. In this mode, the data buffer will accept data via the SPI interface only until the internal FIFO is full (indicated via the transmit ready line going low). The synchronisation word is a CCSDS 32bit Attached Sync Marker (ASM) for non-turbo-coded data: 0x1ACFFC1D.

Precautions

When not transmitting into an antenna, ensure that an appropriate RF load is connected to prevent damaging the transmitter.

4.4 FPGA reset

A reset signal is provided to the header that will allow an external subsystem such as an OBC to reset the FPGA to a known good state. This is an *optional* signal. Alternatively cycling the power of the radio will also reset the FPGA to a known good state.